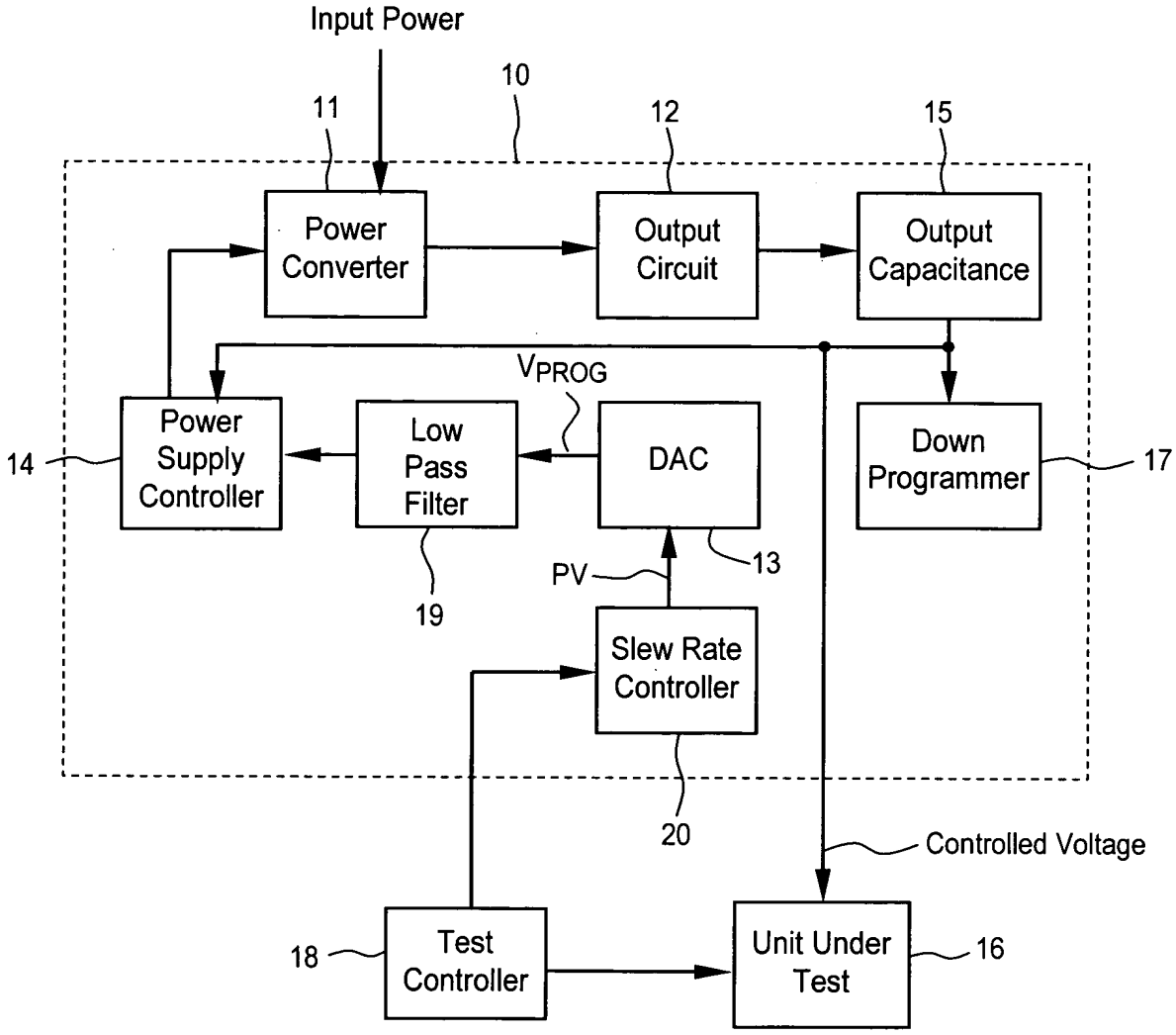
FIG. 1


Input Power
10
11
12
15
Power Converter
Output Circuit
Output Capacitance
VPROG
Power Supply Controller
Low Pass Filter
DAC
Down Programmer
14
17
19
PV
13
Slew Rate Controller
20
Controlled Voltage
18
Test Controller
Unit Under Test
16

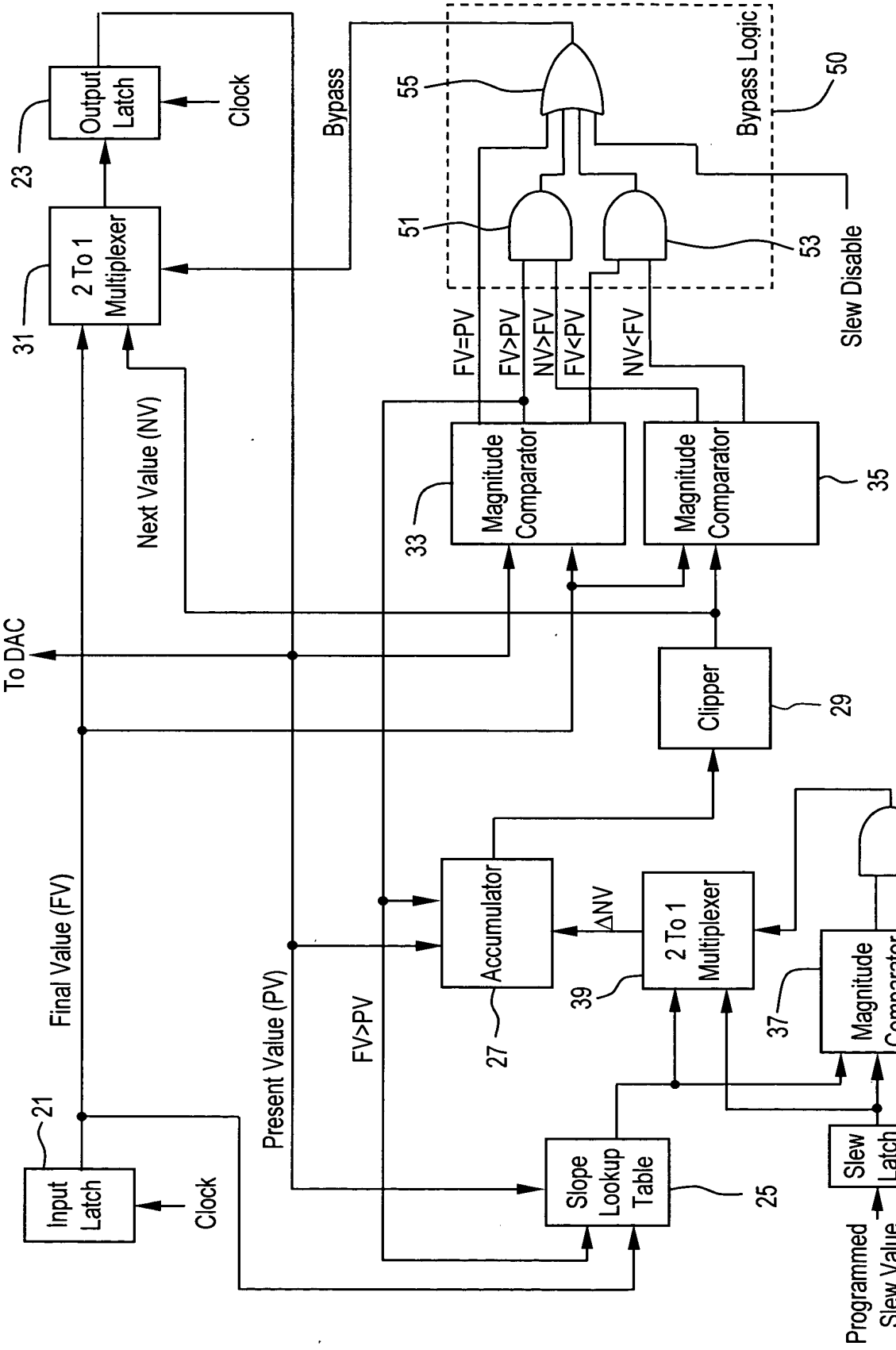

Input Latch
Clock
21
Final Value (FV)
Present Value (PV)
FV>PV
Slope Lookup Table
25
Accumulator
27
ΔNV
2 To 1 Multiplexer
39
Slew Latch
36
Programmed Slew Value
Magnitude Comparator
37
Programmable Slew Enable
41
Clipper
29
To DAC
Next Value (NV)
Magnitude Comparator
33
Magnitude Comparator
35
FV=PV
FV>PV
NV>FV
FV<PV
NV<FV
Bypass Logic
50
55
51
53
Slew Disable
Bypass
2 To 1 Multiplexer
31
Output Latch
23
Clock

FIG. 2

FIG. 3

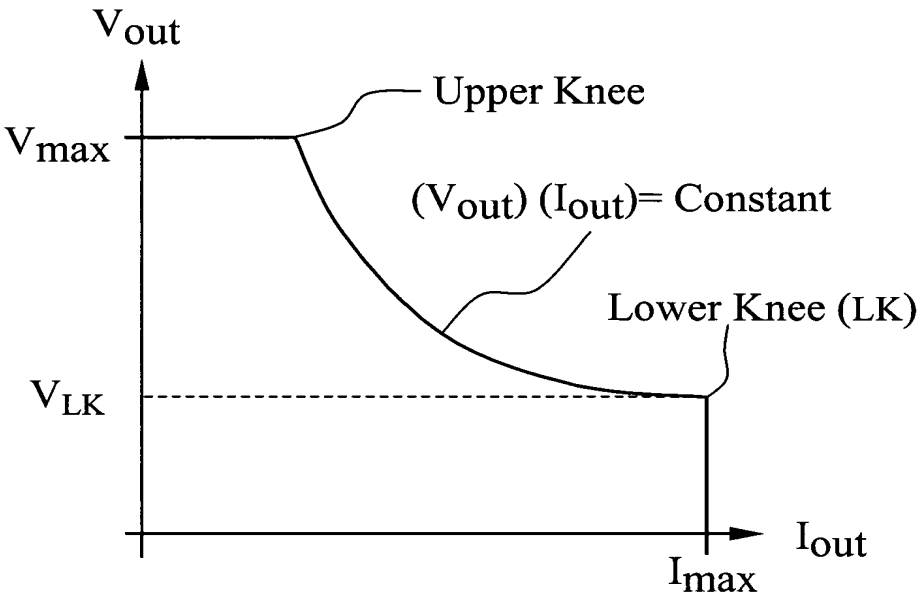


FIG. 4

$$V(t) = V_S + (V_F - V_S)(1 - e^{-t/\tau_1})$$

FIG. 5

$$V(t) = V_S + \left(\frac{V_F^2}{V_{LK}} - V_S\right)(1 - e^{-t/\tau_2})$$

FIG. 6

$$V(t) = \sqrt{V_S^2 + (V_F^2 - V_S^2)(1 - e^{-t/\tau_3})}$$

FIG. 7

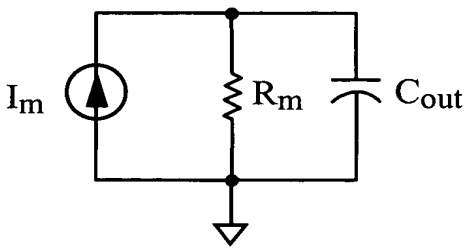


FIG. 8

$$\tau_1 = V_F * C_{out}/I_{max}$$

FIG. 9

$$\tau_2 = V_F^2 * C_{out}/P_{outmax}$$

FIG. 10

$$\tau_3 = V_F^2 * C_{out}/(2 * P_{outmax})$$

FIG. 11

$$V(t) = \sqrt{(V_i^2 - 2P_m * t/C_{out})}$$

FIG. 12

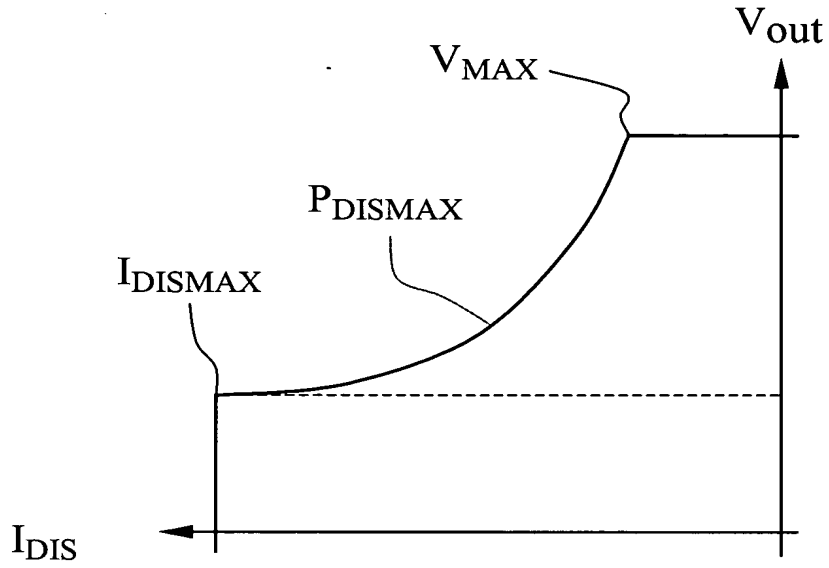

Vout
VMAX
PDISMAX
IDISMAX
IDIS

FIG. 13

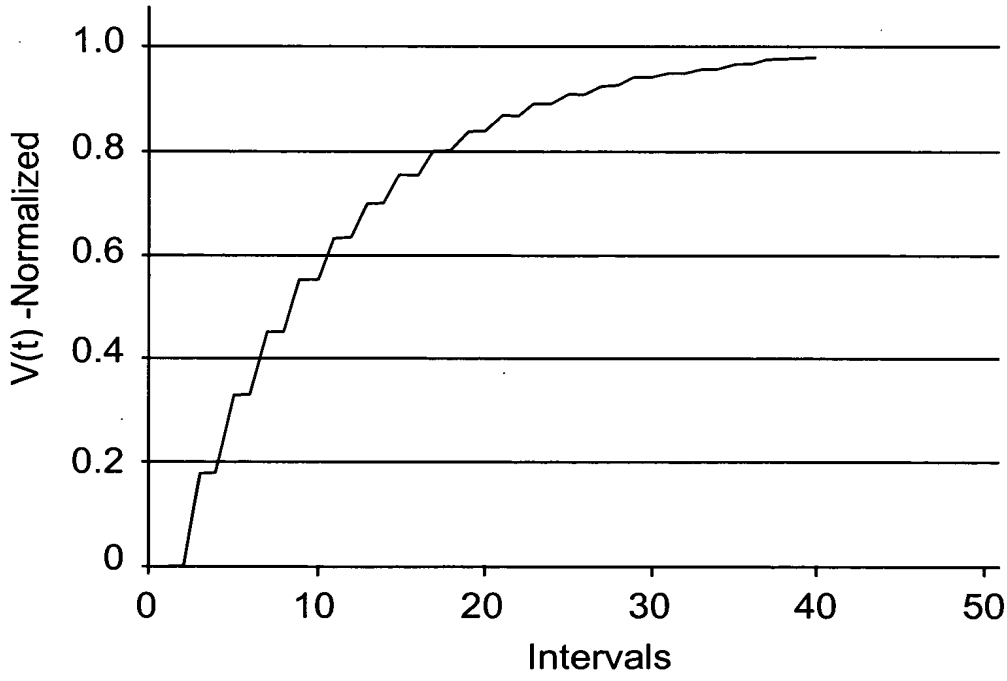

1.0
0.8
0.6
0.4
0.2
0
V(t) -Normalized
0
10
20
30
40
50
Intervals

FIG. 14

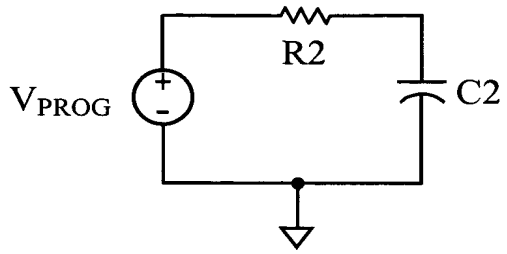
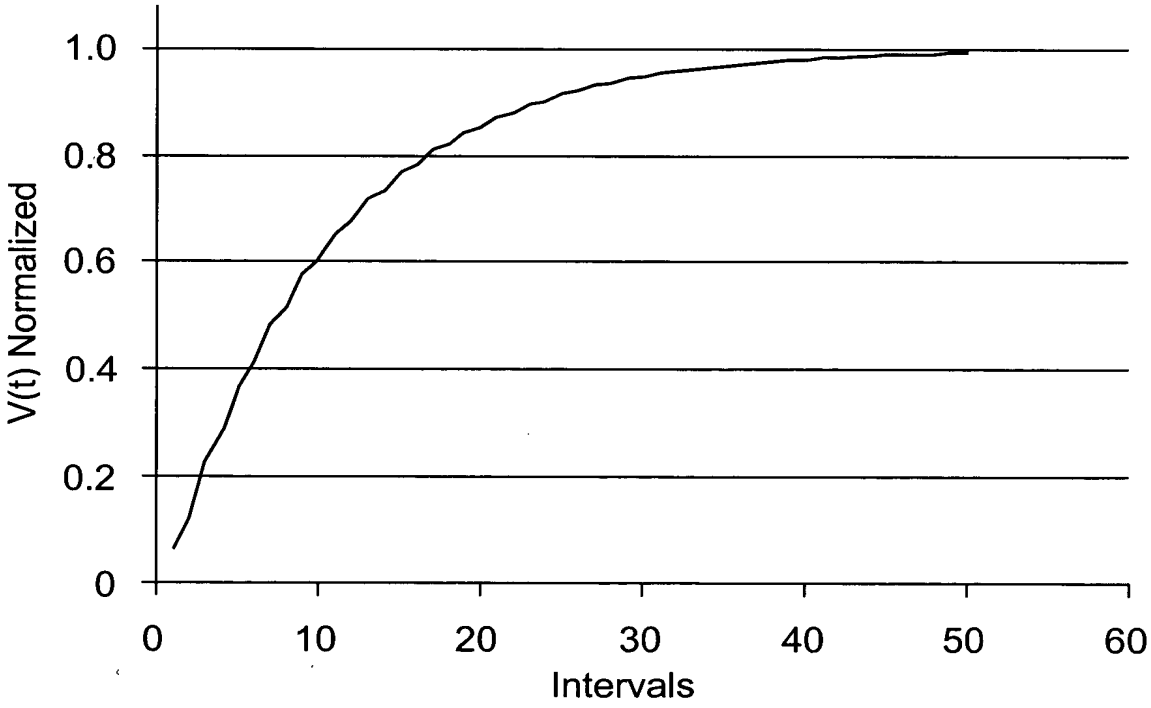

R2
V_{PROG}
+
-
C2

FIG. 15


1.0
0.8
0.6
0.4
0.2
0
V(t) Normalized
0
10
20
30
40
50
60
Intervals